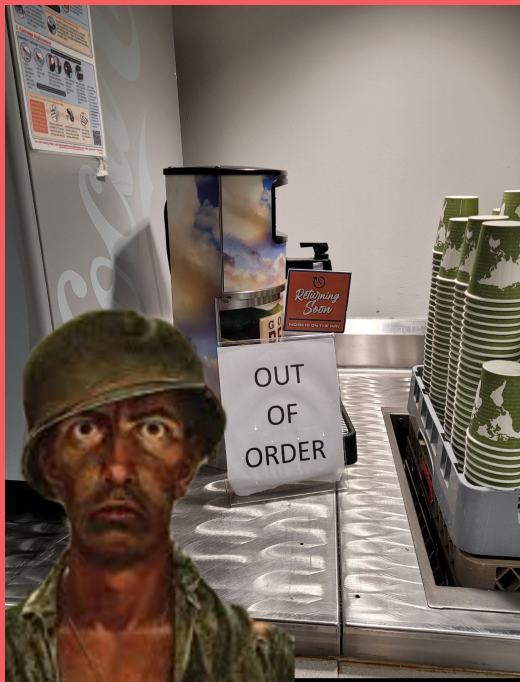


**Welcome back
to BS429H!**

Week B




Ed meme recap:



?? #549

 **Anonymous**
6 days ago in **General**

 PIN  STAR  WATCH 57 VIEWS

 when the matrix can't even comprehend your code
4

Generated at 2024/04/05 22:16, avg score: 612

Test	t0	2	3	4	5	6	7	10	11	12	13	14	15	16	17	18	19	21	22	23	24	25	26	27	28	30	31	32	33	35	36	37	38	39	40	42	43	44	45	46	47	48	49	50	51	52			
Weight	8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
Passing	39	0	12	37	10	33	26	24	34	36	13	36	14	36	11	27	25	15	36	7	34	29	37	37	9	14	36	22	37	14	34	0	36	38	27	32	38	26	29	38	37	0	39	39	37	38			
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Comment Edit Delete Endorse ***

Dawn of
The Final Day
-24 Hours Remain-

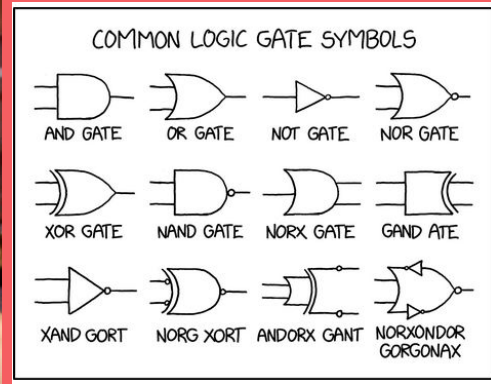


I DON'T KNOW WHAT
misaligned load/store is



AND AT THIS POINT I'M TOO AFRAID
TO ASK

makeameme.org



git clone git@gheith.csres.utexas.edu:cs429h_s24_p9 #582

Anonymous
Yesterday in General

PIN STAR WATCH 50 VIEWS

Due Date:

16 test 4/15/2024 @11:59pm
code 4/17/2024 @11:59pm

Assignment:

- (1) Implement a superscalar processor for a simple instruction set, the ARM AArch64 ISA.
- (2) Contribute a test by adding 2 files and committing them:

```
-<your csid>.hex  your program  
-<your csid>.ok  expected output
```
- (3) Answer the questions in REPORT.txt
- (4) Your grade will be based on performance (CPI) only



me in gtkwave rn (click preview pls) #575

W

W. Cartwright
2 days ago in General

PIN STAR WATCH 57 VIEWS

7

Preview HTML CSS JavaScript

A screenshot of a Spotify playlist preview. The main track is "Whole Lotta Red" by Playboi Carti. Below it, there are three other tracks: "Rockstar Made" by Playboi Carti, "Go2DaMoon (feat. Kanye West)" by Playboi Carti and Kanye West, and "Stop Breathing" by Playboi Carti. The interface is red and includes a play button and a "Save on Spotify" option.

Congrats! You finished all the
assignments!

Questions on lecture content?
Or about cats?

Stress

- 429H is not an easy class
 - Lots of new materials
 - Unfamiliar programming environments
 - Fast, often relentless pace
- Struggling in this course is normal
 - There will be times you won't know the answer of the solution
 - This is expected—we want we everyone to succeed, but the only way we can help is if you ask for it
- If you find yourself overly overwhelmed or spending more time on this class than you think you should be, please reach out to Dr. Gheith or the TAs
 - We can help out as far as the class goes
 - We can provide other resources where we are not able to help

[Mental health resource available at UT](#)

Quiz everyone say **REVIEW!**

Question 1 - Caleb

Total time: 6 hours

Time	0	1	2	3	4	5
Washer 1000	Wash _A	Wash _B	Wash _C	Wash _D	Wash _E	
Dryer 1000		Dry _A	Dry _B	Dry _C	Dry _D	Dry _E

Question 1 - Chris

Total time: 10 hours

Time	0	1	2	3	4	5	6	7	8	9
Washer Dryer 3000	Wash _A	Dry _A	Wash _B	Dry _B	Wash _C	Dry _C	Wash _D	Dry _D	Wash _E	Dry _E

Question 1 - Alex

10 hours vs 11 hours

Time	0	1	2	3	4	5	6	7	8	9
Washer Dryer 4000	Wash _A Dry _A	Wash _B Dry _B	Wash _C Dry _C	Wash _D Dry _D	Wash _E Dry _E	Wash _F Dry _F	Wash _G Dry _G	Wash _H Dry _H	Wash _I Dry _I	Wash _J Dry _J

Time	0	1	2	3	4	5	6	7	8	9	10
Washer 1000	Wash _A	Wash _B	Wash _C	Wash _D	Wash _E	Wash _F	Wash _G	Wash _H	Wash _I	Wash _J	
Dryer 1000		Dry _A	Dry _B	Dry _C	Dry _D	Dry _E	Dry _F	Dry _G	Dry _H	Dry _I	Dry _J

Question 1 - Willow & Jocelyn

Total time: 7.5 hours

Time	0	1	2	3	4	5	6	7
Washer 1000	Wash _A ¹ Wash _A ²	(wait) Wash _C ¹	Wash _C ² (wait)	Wash _E ¹ Wash _E ²	(wait) Wash _G ¹	Wash _G ² (wait)	Wash _I ¹ Wash _I ²	
Washer Dryer 4000	Wash _B Dry _B	Dry _A Wash _D	Dry _D Dry _C	Wash _F Dry _F	Dry _E Wash _H	Dry _H Dry _G	Wash _J Dry _J	Dry _I

Question 2

```
begin_of_while:
    mov $1, i
begin_of_for:
    code for inside of for loop
    add $1, i
    cmp i, $5
    jl begin_of_for //i at this point, before jump
    jmp begin_of_while
```

i=2	i=3	i=4	i=5	i=2	i=3	i=4	i=5	i=2
00	01	10	11	10	11	11	11	10

Question 3

Dr. Gheith created the following Verilog module to perform the addition of two different integers. Propose three different inputs (don't just swap *a_in* and *b_in*) for *a_in* and *b_in* that effectively test the module? Explain why you selected these inputs?

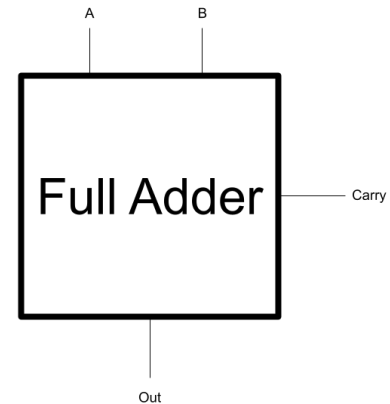
```
module addition (input [7:0] a_in, input [7:0] b_in, output [7:0] out);
```

Question 3

Dr. Gheith created the following Verilog module to perform the addition of two different integers. Propose three different inputs (don't just swap a_in and b_in) for a_in and b_in that effectively test the module? Explain why you selected these inputs?

```
module addition (input [7:0] a_in, input [7:0] b_in, output [7:0] out);
```

<i>a_in</i>	<i>b_in</i>
11111111	11111111
11111111	00000001
11111111	00000000
00000000	00000000



Question 4

```
0: mov $1, %rax
1: mov $2, %rbx
2: add %rax, %rbx
3: mov (%rdx), %rcx
4: sub %rcx, %rbx // rbx = rbx - rcx
5: jmp on_a_trampoline
   on_a_trampoline:
6: mov %rax, (%rdx)
7: mov %rbx, (%rdx, $0x10)
8: mov %rcx, (%rdx, $0x20)
9: jnz %rsi, the_abyss
```

0	
1	
2	0,1
3	
4	2,3
5	
6	0, 3 (WaR), 5 (control dependency)
7	4, 5
8	3, 5
9	5

Question 4

- b. Assume that an instruction is evaluated in a single-cycle. How many cycles will a standard single-cycle processor take to complete this code (i.e. resolve the last jump)?

10

- c. Now also assume that all instructions are executed simultaneously when possible. How many cycles will an out-of-order processor take?

4

Final Project

Final Project Info!

- work in groups of **up to four people**
- presentations will be April 25th and April 26th
 - presentation scheduling is up to y'all to organize
 - project final submission will be due April 29
- anything architecture related
 - extend a project we already did
 - something completely new
- project proposal - more info next slide
- p9 will likely ask for similar elements included in the proposal, plus any research or proof of concept
- form groups + ideas **now**

Project Proposals

- Due April 15th at 11:59pm
- Submit by making a **public** post on Ed Discussion
- Mention if you are looking for additional group members
- Feel free to leave positive comments or questions on others' proposals
- Tag proposals with "Project Proposal" tag
- Title: <team name> - <project name>
- Include team members, description of the project, timeline, and questions you might have

Example

Team Members: Caleb Eden, Chris Hill, ~~Alex Huang, Willow Stenglein~~, Jocelyn Zhang

Proposed work: Teach the freshmen about cats

Timeline:

4/19: Research cat facts and locate cats

4/26: Take pictures of cats and start on presentation

4/29: Finish presentation; share with world

Questions:

Are we allowed to bring a cat into discussion?

What we are looking for in presentation

- Be prepared!!
 - Have a backup plan if your live demo doesn't work
- Explain your work
 - Provide background that is appropriate for CS429H students
 - Ideally people will learn something about architecture from your presentation!
- Demonstrate what you did
 - Show screenshots of results, live demos, whatever is appropriate for your project

Final Project Ideas !!!

- We have posted a long list of project ideas on Ed
- Note: We have 2 FPGAs (maybe more) so please let us (and probably more importantly Gheith) know early if you'll want one!

Questions?

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